Power Management ICs for Automotive Body Control

LED Drivers for Automotive Light

BD8381EFV-M

No.11039EAT14

●Description

BD8381EFV-M is a white LED driver with the capability of withstanding high input voltage (50V MAX).
A current-mode buck-boost DC/DC controller is also integrated to achieve stable operation against voltage input and also to remove the constraint of the number of LEDs in series connection.
The brightness can be controlled by either PWM or DC. The PWM brightness signal generation circuit is built into, and the control without microcomputer is also possible.

●Features

1) Input voltage range 5.0 – 30 V
2) Integrated buck-boost current-mode DC/DC controller
3) Built-in CR timer for PWM brightness
4) PWM linear brightness
5) Built-in protection functions (UVLO, OVP, TSD, OCP, SCP)
6) LED error status detection function (OPEN/ SHORT)
7) HTSSOP-B28 package

●Applications

Headlight and running (DRL) of night of daylight, etc.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Power supply voltage	VCC	50	V
BOOT Voltage	V_{BOOT}	55	V
SW,CS,OUTH Voltage	V_{SW}, V_{CS}, V_{OUTH}	50	V
BOOT-SW Voltage	$V_{BOOT-SW}$	7	V
VREG,OVP,OUTL,FAIL1,FAIL2,THM,SS, COMP,RT,SYNC,EN,DISC,VTH,FB,LEDR, LEDC,DRLIN, PWMOUT,CT Voltage	V_{VREG},V_{OVP},V_{OUTL},V_{FAIL1},V_{FAIL2},V_{THM},V_{SS}, V_{COMP},V_{RT},$V_{SYNC}$$V_{EN}$,$V_{DISC}$,$V_{VTH}$,$V_{FB}$,$V_{LEDR}$, V_{LEDC}, ,V_{DRLIN},V_{PWMOUT} V_{CT}	-0.3～7 < V_{CC}	V
Power Consumption	Pd	1.45※1	W
Operating temperature range	Topr	-40～+125	℃
Storage temperature range	Tstg	-55～+150	℃
Junction temperature	Tjmax	150	℃

※1 IC mounted on glass epoxy board measuring 70mm×70mm×1.6mm, power dissipated at a rate of 11.6mW/℃ at temperatures above 25℃.
※2 A radiation is not designed.

●Operating conditions (Ta=25℃)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	5.0～30	V
Oscillating frequency range	F_{OSC}	200～600	kHz
External synchronization frequency range ※3 ※4	F_{SYNC}	fosc～600	kHz
External synchronization pulse duty range	F_{SDUTY}	40～60	%

※3 Connect SYNC to GND or OPEN when not using external frequency synchronization.
※4 Do not switch between internal and external synchronization when an external synchronization signal is input to the device.

●**Electrical characteristics** (Unless otherwise specified, VCC=12V Ta=25℃)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max.		
Circuit current	ICC	-	4.5	7.0	mA	EN=Hi, SYNC=Hi, RT=OPEN, CIN=10μF
Standby current	IST	-	0	8	μA	EN=Low
[VREG Block (VREG)]						
Reference voltage	VREG	4.5	5.0	5.5	V	IREG=-5mA, CREG=10μF
[OUTH Block]						
OUTH high-side ON resistance	RONHH	1.5	3.5	7.0	Ω	ION=-10mA
OUTH low-side ON resistance	RONHL	1.0	2.5	5.0	Ω	ION=10mA
Over-current protection operating voltage	VOLIMIT	VCC -0.68	VCC -0.60	VCC -0.52	V	
[OUTL Block]						
OUTL high-side ON resistance	RONLH	2.0	4.0	8.0	Ω	ION=-10mA
OUTL low –side ON resistance	RONLL	1.0	2.5	5.0	Ω	ION=10mA
[SW Block]						
SW low -side ON resistance	RONSW	2.0	4.5	9.0	Ω	IONSW=10mA
[PWMOUT Block]						
PWMOUT high-side ON resistance	RONPWMH	2.0	4.0	8.0	Ω	IONPWMH=-10mA
PWMOUT low-side ON resistance	RONPWML	1.0	2.5	5.0	Ω	IONPWML=10mA
[Error Amplifier Block]						
Reference voltage	VREF2	0.190	0.200	0.210	V	FB-COMPShort, Ta=-40℃～125℃
COMP sink current	ICOMPSINK	50	75	100	μA	VFB>0.2V, Vcomp=1V
COMP source current	ICOMPSOURCE	-100	-75	-50	μA	VFB <0.2V, Vcomp=1V
[Oscillator Block]						
Oscillating frequency	FOSC	285	300	315	KHz	RT=100kΩ
[OVP Block]						
Over-voltage detection reference voltage	VOVP	1.9	2.0	2.1	V	VOVP=Sweep up
OVP hysteresis width	VOHYS	0.45	0.55	0.65	V	VOVP= Sweep down
[UVLO Block]						
UVLO voltage	VUVLO	4.0	4.3	4.6	V	VCC : Sweep down
UVLO hysteresis width	VUHYS	50	150	250	mV	VCC : Sweep up
[PWM Generation circuit Block]						
VTH Threshold voltage	VTH1	3	2/3VREG	3.7	V	
VTH Threshold voltage	VTH2	1	1/3VREG	2	V	
PWM minimum ON width	TPWMON	25	-	-	μs	
LED OPEN detection function	VOPEN	30	50	70	mV	
LED SHORT detection function	VSHORT	100	200	400	mV	VSHORT≧IVLEDR-VLEDCI
LED GND short protection timer	TSHORT	100	150	200	ms	CT=0.1μF
[Logic Inputs]						
Input HIGH voltage	VINH	3.0	-	-	V	
Input LOW voltage	VINL	GND	-	1.0	V	
Input current 1	IIN	20	35	50	μA	VIN=5V (SYNC/DRLIN)
Input current 2	IEN	25	40	55	μA	VEN=5V (EN)
[FAIL Output (open drain)]						
FAIL LOW voltage	VOL	-	0.1	0.2	V	IOL=0.1mA

◎ This product is not designed for use in radioactive environments.

●Electrical characteristic curves (Reference data)

(Unless otherwise specified, Ta=25℃)

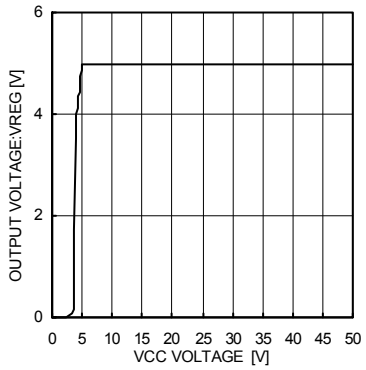


Fig.1 VREG Temperature characteristic

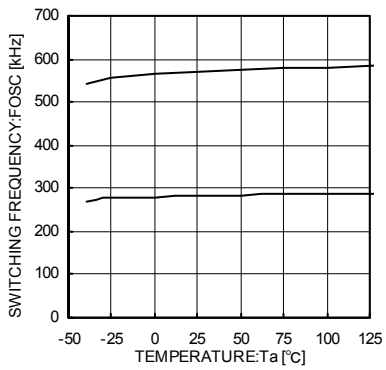


Fig.2 OSC Temperature characteristic

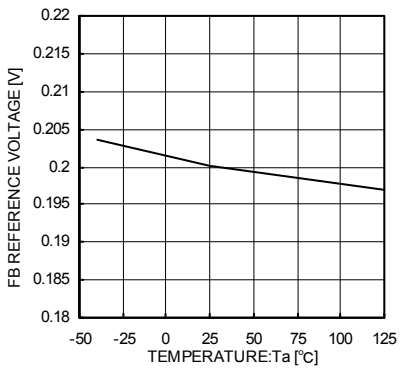


Fig.3 Standard voltage temperature characteristic

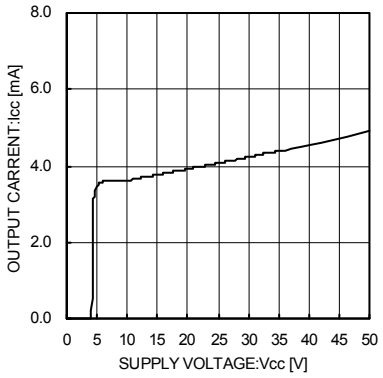


Fig.4 Circuit current (Switching OFF)

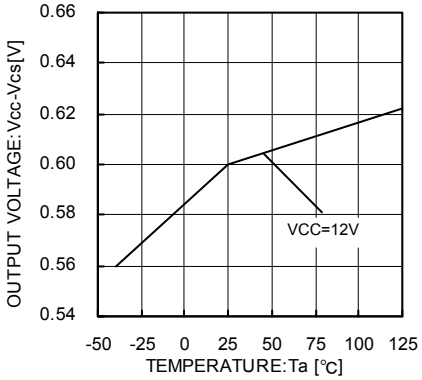


Fig.5 Overcurrent detection voltage temperature characteristic

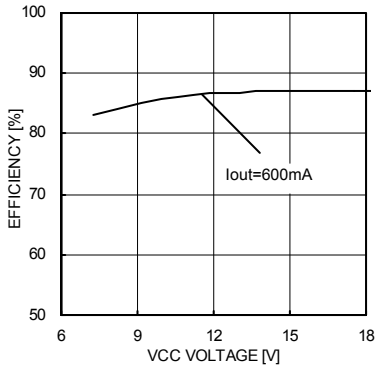


Fig.6 Efficiency (Input voltage dependence)

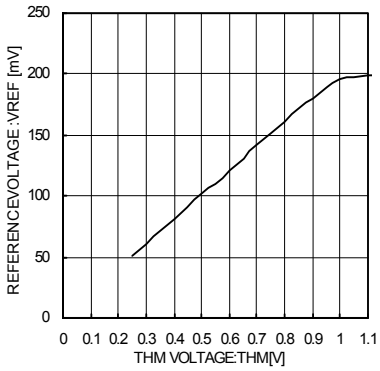


Fig.7 THM Gain

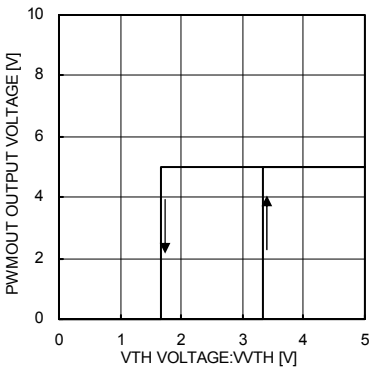


Fig.8 VTH Threshold voltage

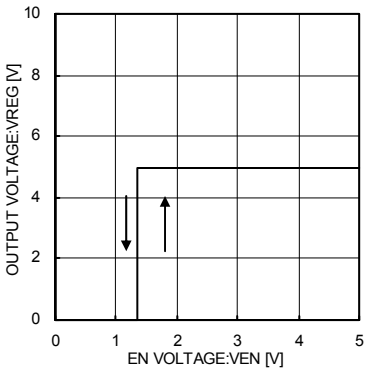


Fig.9 EN Threshold voltage

●Block diagram and pin configuration

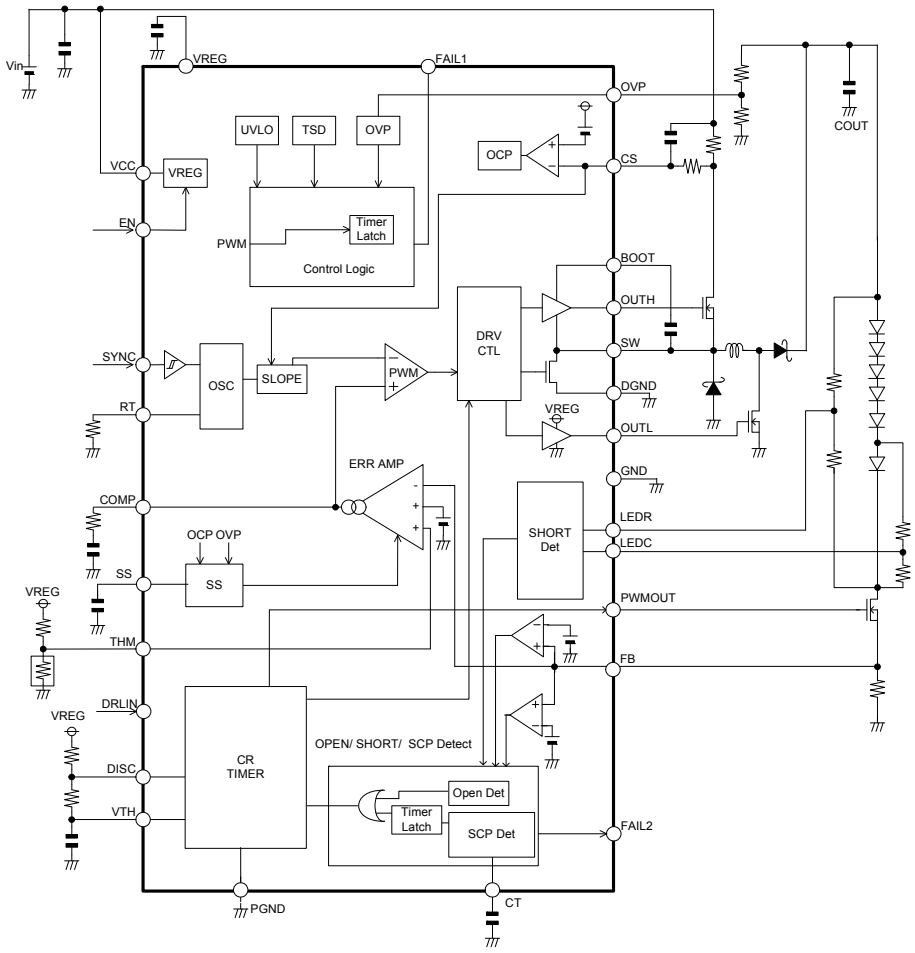


Fig.10 Buck-boost application composition

●Pin layout

BD8381EFV-M(HTSSOP-B28)

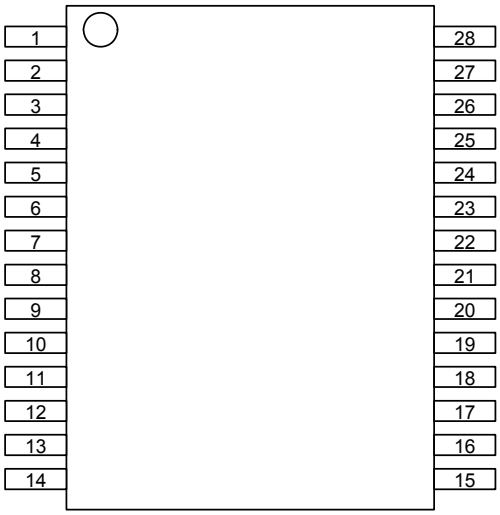


Fig.11

●Pin function table

Pin	Symbol	Function
1	COMP	Error amplifier output
2	SS	Soft start
3	VCC	Input power supply
4	EN	Enable input
5	RT	Oscillation frequency-setting resistance input
6	SYNC	External synchronization signal input
7	GND	Small-signal GND
8	THM	Thermally sensitive resistor connection pin
9	FB	ERRAMP FB signal input pin
10	DISC	CR Timer discharge pin
11	VTH	CR Timer threshold pin
12	DRLIN	DRL switch terminal (Pulse output setting terminal)
13	FAIL1	Failure signal output
14	FAIL2	LED open/short detection signal output
15	OVP	Over-voltage detection input
16	LEDC	LED short detection pin (LED detection side)
17	LEDR	LED short detection pin (Resistor detection side)
18	N.C.	-
19	PGND	PWM brightness source pin
20	PWMOUT	PWM brightness signal output pin
21	CT	GND short protection timer setting pin
22	OUTL	Low-side external FET Gate Drive out put
23	DGND	Low-side FET driver source pin
24	SW	High-side FET Source pin
25	OUTH	High-side external FET Gate Drive out put
26	CS	DC/DC output current detection pin
27	BOOT	High-side FET driver source pin
28	VREG	Internal reference voltage output

●5V voltage reference (VREG)

5V (Typ.) is generated from the VCC input voltage when the enable pin is set high. This voltage is used to power internal circuitry, as well as the voltage source for device pins that need to be fixed to a logical HIGH.
UVLO protection is integrated into the VREG pin. The voltage regulation circuitry operates uninterrupted for output voltages higher than 4.5 V (Typ.), but if output voltage drops to 4.3 V (Typ.) or lower, UVLO engages and turns the IC off.
Connect a capacitor (Creg = 10μF Typ.) to the VREG terminal for phase compensation. Operation may become unstable if Creg is not connected.

●About the method of setting the output current

ILED=min[THM / 5 V , 0.2V] / RISET [A]
As for min[THM / 5 V, 0.2V], small one is selected from among THM and VFB=0.2V.
Please input within the range of 0.25-5.0V when controlling the output current with THM. Please connect with VREG when not using THM. There is a possibility that the LED GND short detection malfunctions when THM≦0.25V.
As for PWM brightness, the control by the PWM signal from the outside and brightness with the CR timer are possible.
(GND short protection detection timer (SCP) works at the same time as turning on EN when PWM brightness from the outside is used. Therefore, there is a possibility of mis-detecting SCP for the time from the EN turning on to the PWM turning on > GND short protection detection timer.)

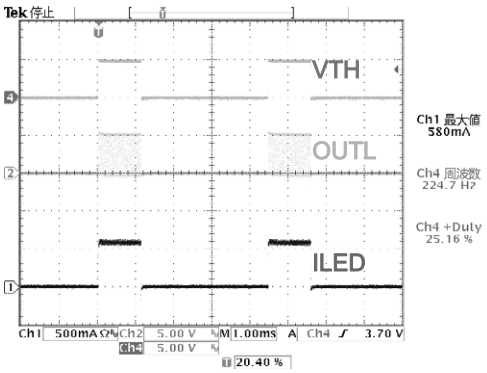


Fig. 12

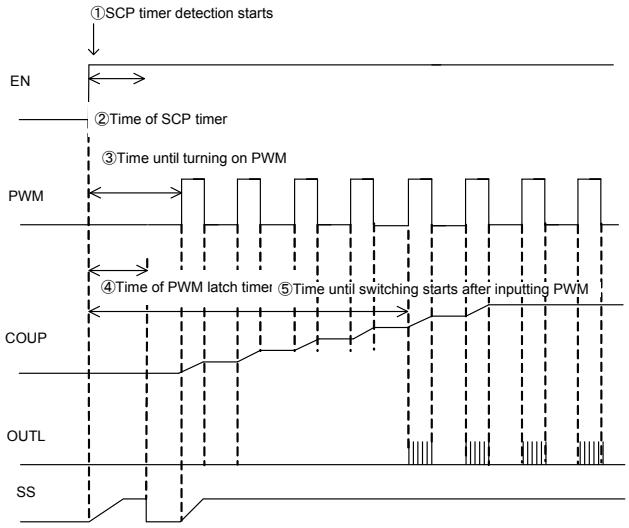
Rcr1	20	kΩ
Rcr2	10	kΩ
Ccr	100000	pF

$$FPWM=\frac{1.44}{(RCR1+2RCR2)CCR}$$

$$TON\_PWM=\frac{RCR2}{(RCR1+2RCR2)}\times 100$$

●About time from EN turning on to PWM turning on and the start from PWM low Duty

※The GND short protection detecting function (hereafter, SCP) starts with EN=Low→Hi, and after the time of the timer set with the external capacitor connected with CT, it becomes latch off. (Above figure ① and ②)
The charge with SS begins synchronizing with turning on EN. The PWM latch off function is built into when there is not PWM turning on, and when the PWM latch off is detected, (② of SS and the SCP counter) is reset. (The time of the timer at latch OFF is calculated by oscillatory frequency ×32770 counts of DC/DC.) Therefore, the following relations exist at time until PWM is turned on, time of PWM latch timer and SCP detection time after EN is turned on at external brightness.
(However, after ③ is turned on, ③ <④ is deleted from the sequence because ④ doesn't operate.)
Each sequence
②＜④＜③⇒SCP is detected and No LED light.
④＜②＜③⇒LED lighting
④＜③＜②⇒LED lighting



●About Dirating of the LED current that uses THM

It is an ability to set the Dirating curve of the LED current to the temperature as one of the functions to use THM. As for LED, because deterioration at the high temperature is fast, the maximum allowance LED currents and the curve of temperatures is given to the data sheet of LED. The voltage with a negative temperature characteristic in THM the Thermistor resistance is used is input, and the LED current is controlled when the LED current is controlled according to the temperature characteristic. Moreover, external Tr is used, and two input composition is also possible.

●Buck-Boost DC/DC controller

・Over-voltage protection circuit (OVP)

The output of the DCDC converter should be connected to the OVP pin via a voltage divider. In determining an appropriate trigger voltage of for OVP function, consider the total number of LEDs in series and the maximum variation in VF. Also, bear in mind that over-current protection (OCP) is triggered at 0.85 x OVP trigger voltage. If the OVP function engages, it will not release unless the DCDC voltage drops to 72.5% of the OVP trigger voltage. For example, if ROVP1 (out put voltage side), ROVP2 (GND side), and DCDC voltage VOUT are conditions for OVP, then:

VOUT ≥ (**ROVP1** + **ROVP2**) / **ROVP2** x **2.0** V.

OVP will engage when **VOUT** ≧ **32** V if **ROVP1** = **330** kΩ and **ROVP2** = **22** kΩ.

・Buck-boost DC/DC converter oscillation frequency (FOSC)

The regulator's internal triangular wave oscillation frequency can be set via a resistor connected to the RT pin (pin 5). This resistor determines the charge/discharge current to the internal capacitor, thereby changing the oscillating frequency. Refer to the following theoretical formula when setting RT:

$$fosc = \frac{60 \times 10^6}{RT\,[\Omega]} \times \alpha \ [kHz]$$

60×10^6 (V/A/S) is a constant (±5%) determined by the internal circuitry, and α is a correction factor that varies in relation to RT:
{ RT: α = 50kΩ: 0.98, 60kΩ: 0.985, 70kΩ: 0.99, 80kΩ: 0.994, 90kΩ: 0.996, 100kΩ: 1.0,
150kΩ: 1.01, 200kΩ: 1.02, 300kΩ: 1.03, 400kΩ: 1.04, 500kΩ: 1.045 }

A resistor in the range of 62.6kΩ～523kΩ is recommended. Settings that deviate from the frequency range shown below may cause switching to stop, and proper operation cannot be guaranteed.

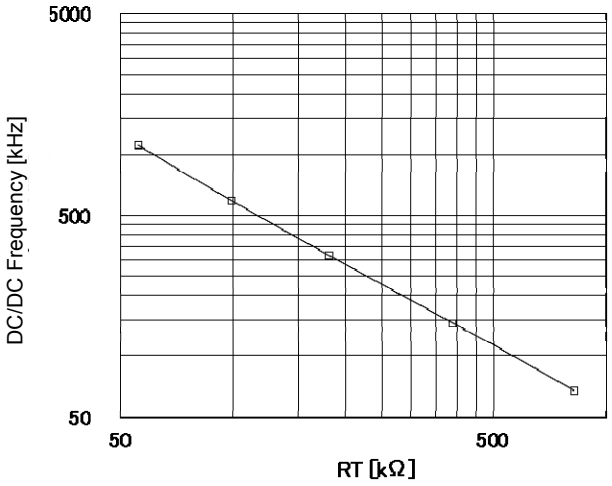


Fig.13 RT versus switching frequency

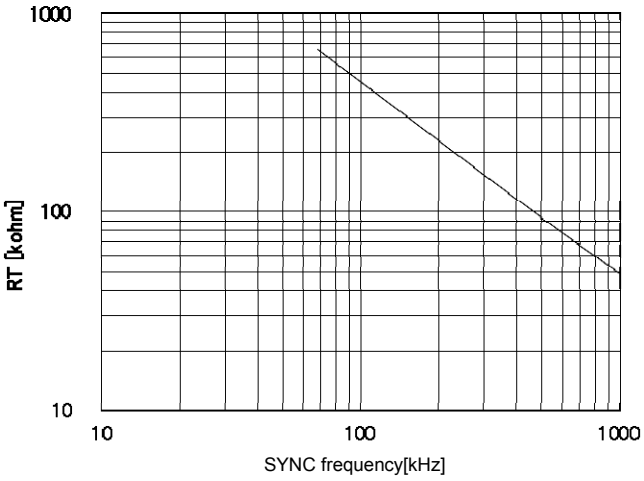


Fig.14 RT versus SYNC frequency

・External DC/DC converter oscillating frequency synchronization (FSYNC)

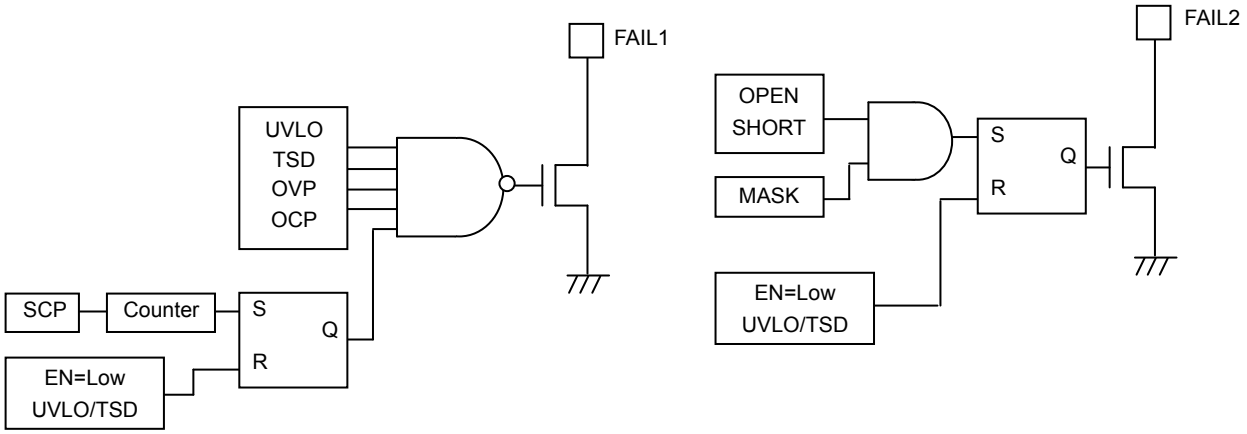
Do not switch from external to internal oscillation of the DC/DC converter if an external synchronization signal is present on the SYNC pin. When the signal on the SYNC terminal is switched from high to low, a delay of about 30 μs (typ.) occurs before the internal oscillation circuitry starts to operate (only the rising edge of the input clock signal on the SYNC terminal is recognized). Moreover, the external synchronizing signal is given to priority when an external input frequency is used. And in the case of using external input frequency, follow the Fig.14.

・Soft Start Function

The soft-start (SS) limits the current and slows the rise-time of the output voltage during the start-up, and hence leads to prevention of the overshoot of the output voltage and the inrush current. The SS voltage is made Low when OVP of the overcurrent and the excess voltage is detected, and the switching is stopped. Resume operation is begun.

・Self-diagnostic functions

The operating status of the built-in protection circuitry is propagated to FAIL1 and FAIL2 pins (open-drain outputs). FAIL1 becomes low when UVLO, TSD, OVP, or SCP protection is engaged, whereas FAIL2 becomes low when open or short LED is detected.



・Operation of the Protection Circuitry

・Under-Voltage Lock Out (UVLO)

The UVLO shuts down all the circuits other than REG when VREG ≦ 4.3V (TYP).

・Thermal Shut Down (TSD)

The TSD shuts down all the circuits other than REG when the Tj reaches 175℃ (TYP), and releases when the Tj becomes below 150℃ (TYP).

・Over Current Protection (OCP)

The OCP detects the current through the power-FET by monitoring the voltage of the high-side resistor, and activates when the CS voltage becomes less than VCC-0.6V (TYP).

When the OCP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.

・Over Voltage Protection (OVP)

The output voltage of the DCDC is detected with the OVP-pin voltage, and the protection activates when the OVP-pin voltage becomes greater than 2.0V (TYP).

When the OVP is activated, the external capacitor of the SS pin becomes discharged and the switching operation of the DCDC turns off.

・Short Circuit Protection (SCP)

When the FB-pin voltage becomes less than 0.05V (TYP), the internal counter starts operating and latches off the circuit approximately after 150ms (when CT = 0.1μF). If the FB-pin voltage becomes over 0.05V before 150ms, then the counter resets. When the LED anode (i.e. DCDC output voltage) is shorted to ground, then the LED current becomes off and the FB-pin voltage becomes low. Furthermore, the LED current also becomes off when the LED cathode is shorted to ground. Hence in summary, the SCP works with both cases of the LED anode and the cathode being shorted.

・LED Open Detection

When the LED-pin voltage ≤ 0.05V (TYP) as well as OVP-pin voltage ≥ 1.7V (TYP) simultaneously, the device detects as LED open and latches off that particular channel.

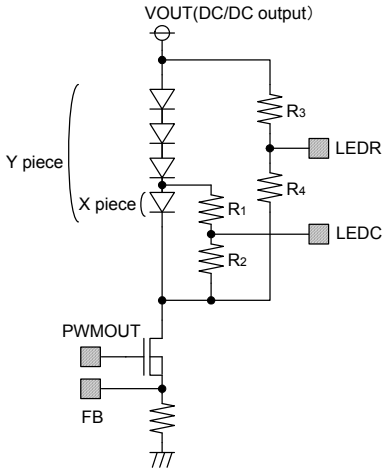
・LED Short Detection

When the voltage between LEDR-pin and LEDC-pin ≥ 0.2 (TYP), the internal counter starts operating, and approximately after 100ms (when FOSC = 300kHz) the operation latches off. With the PWM brightness control, the detecting operation is processed only when PWMOUT-pin = High. If the condition of the detection operation is released before 100ms (when FOSC = 300kHz), then the internal counter resets.

There is a possibility that the LED short detection malfunctions when the difference of Vf is large. Therefore, please adjust external resistance for connected Vf. It is recommended 2V-3V to the input range of LEDR and LEDC.

※The counter frequency is the DCDC switching frequency determined by the RT. The latch proceeds at the count of 32770.

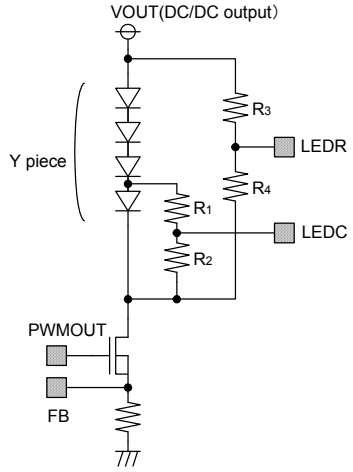
○High luminance LED (multichip) with built-in LED of X piece in 1chip when using Y piece



Setting method
R1 : R2 = X : 1
R3 : R4 = (X + 1) Y – 1 : 1

Fig. 15

○When using the single chip



Setting method
R1 : R2 = 1 : 1
R3 : R4 = 2Y – 1 : 1

Fig. 16

●Error all condition

Protection	Detecting Condition		Operation after detect
	[Detect]	[Release]	
UVLO	VREG<4.3V	VREG>4.45V	All blocks (but except REG) shut down
TSD	Tj>175℃	Tj<150℃	All blocks (but except REG) shut down
OVP	VOVP>2.0V	VOVP<1.45V	SS discharged
OCP	VCS≦VCC-0.6V	VCS>VCC-0.6V	SS discharged
SCP	VFB<0.05V (150ms delay when CT=0.1μF)	EN or UVLO	Counter starts and then latches off all blocks (but except REG)
LED open	VFB<0.05V & VOVP>1.7V	EN or UVLO	Counter starts and then latches off all blocks (but except REG)
LED short	IVLEDR-VLEDCI>0.2V (100ms delay when FOSC=300kHz)	EN or UVLO	Counter starts and then latches off all blocks (but except REG)

●Protection sequence

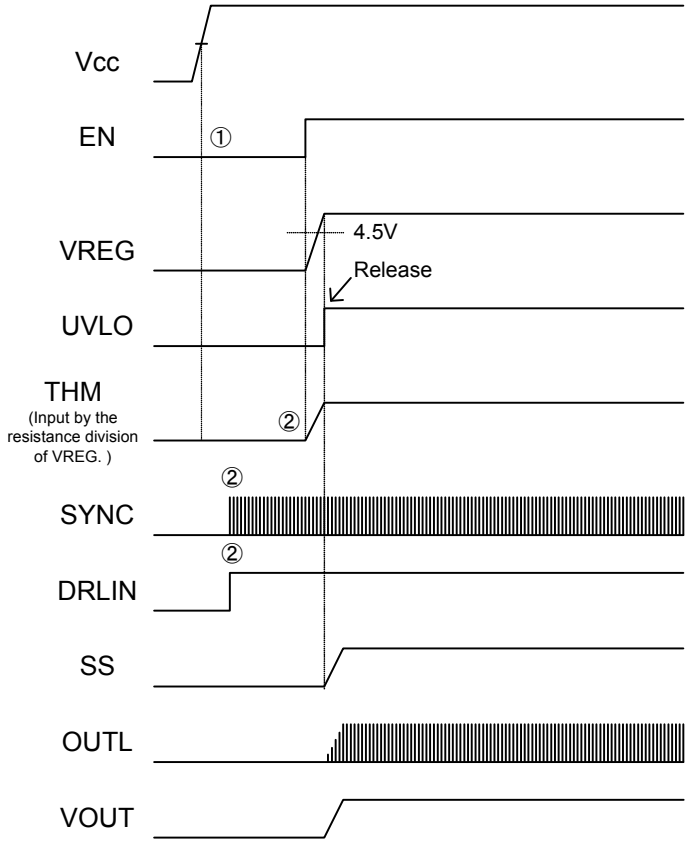


Fig.17

Power supply turning on sequence
① Please turn on EN with Vcc≧4.5V or more after impressing Vcc.
② Please fix the potential of DRLIN and THM before turning on EN.
③ A soft start operates at the same time as turning on EN, and the switching is output.
④ After turning on VCC, the order is not related to other input when inputting external PWM from VTH.）
※It leads to the destruction of IC and external parts because it doesn't error output according to an external constant of adjacent pin 24pin SW terminal, 25pin OUTH terminal, 26pin CS terminal and 27pin BOOT terminal.

●Operation in error circumstances of LED

① LED open detection

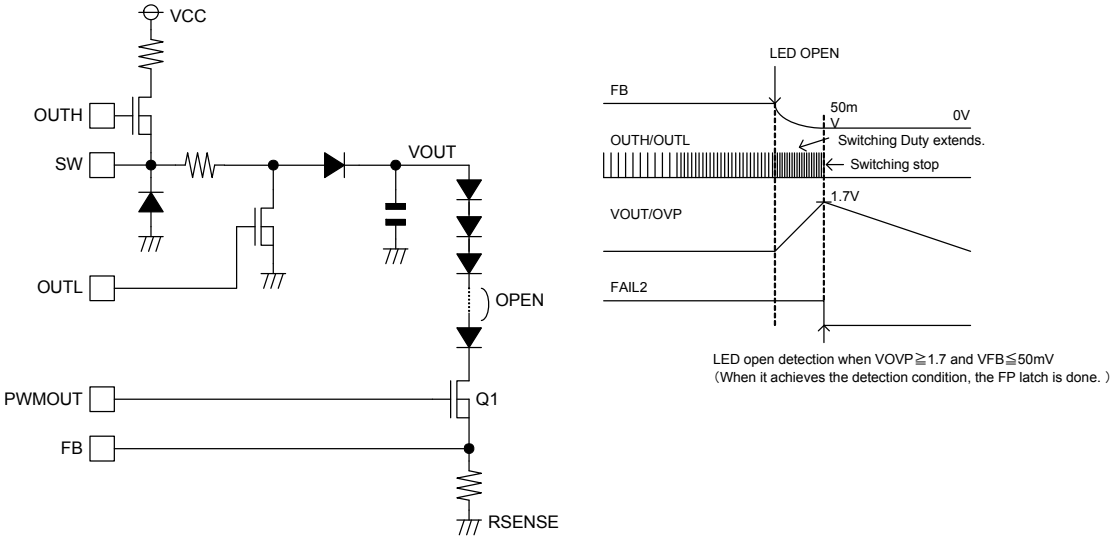


Fig.18

②LED short detection

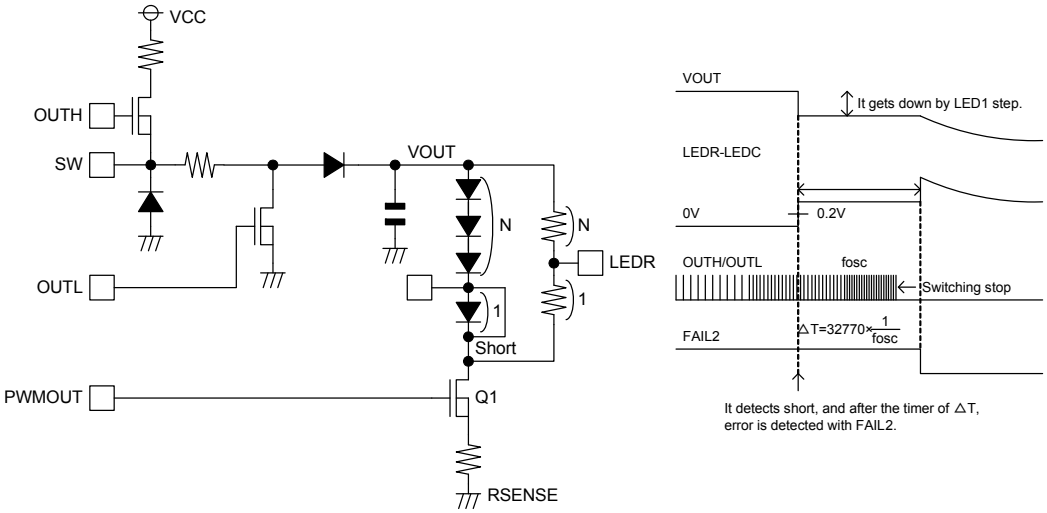


Fig.19

③ LED anode/cathode land GND short detection

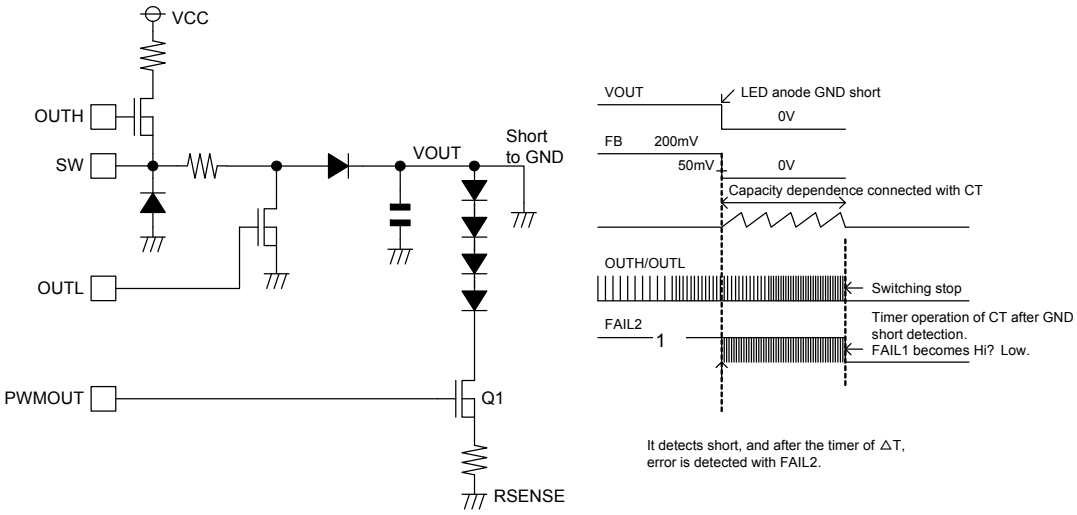
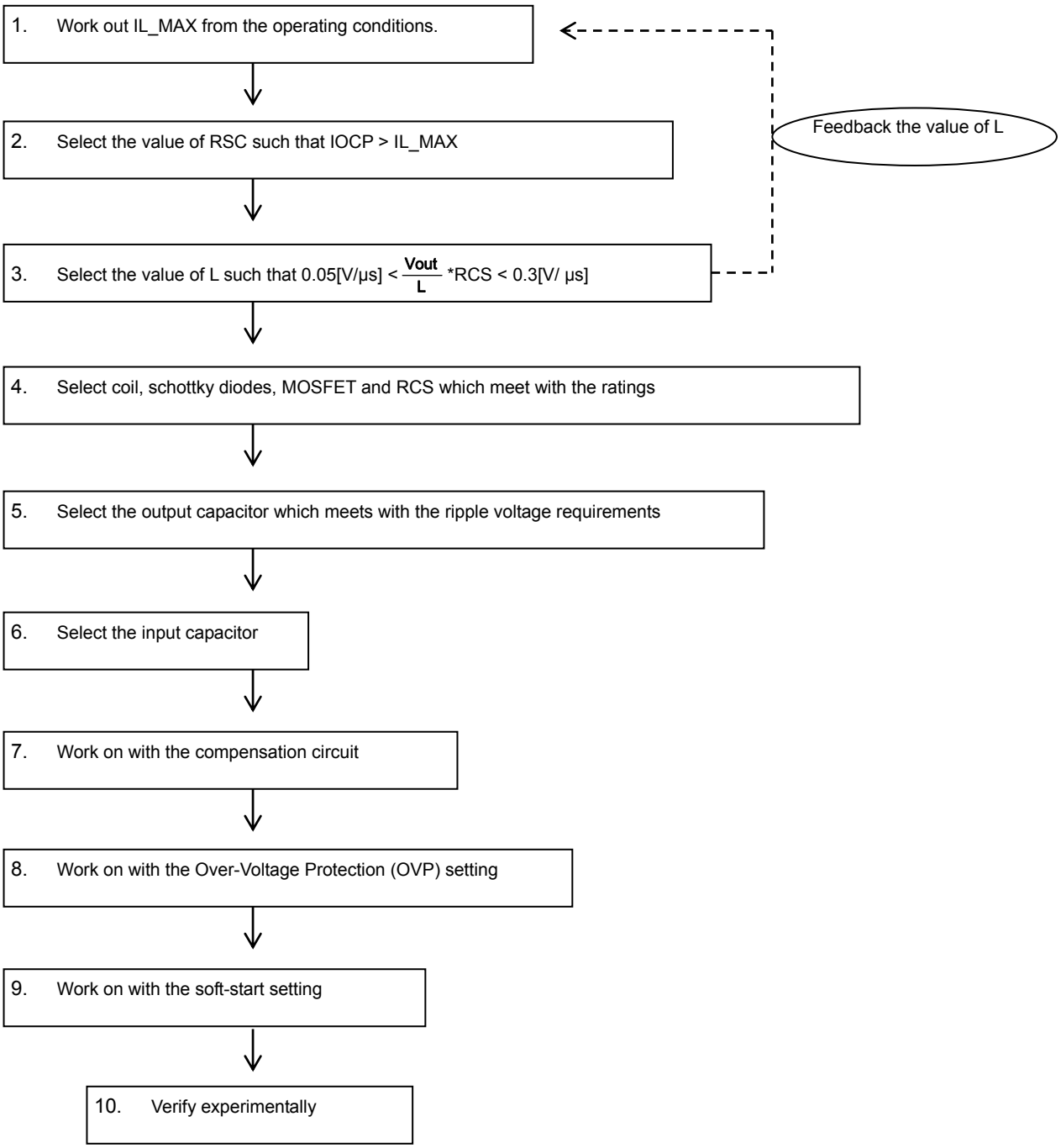


Fig.20

●Procedure for external components selection

Follow the steps as shown below for selecting the external components



1. Computation of the Input Peak Current and IL_MAX

①Calculation of the maximum output voltage (Vout_max)

To calculate the Vout_max, it is necessary to take into account of the VF variation and the number of LED connection in series.

Vout_max = (VF + ΔVF) × N + 0.2+ RPWMON × Iout ΔVF: VF Variation N: Number of LED connection in series

RPWMON: PWMOUT FET Ron

②Calculation of the output current Iout

$$Iout = \frac{0.2V}{RISET}$$

D: FB standard voltage variation

M: Output current resistance variation

③Calculation of the input peak current IL_MAX

IL_MAX = IL_AVG + 1/2 ΔIL

IL_AVG = (VIN + Vout) × Iout / (n × VIN)

$$\Delta IL = \frac{VIN}{L} \times \frac{1}{Fosc} \times \frac{Vout}{VIN+Vout}$$

n: efficiency Fosc: switching frequency

- The worst case scenario for VIN is when it is at the minimum, and thus the minimum value should be applied in the equation.
- The L value of 10μH ~ 47μH is recommended. The current-mode type of DC/DC conversion is adopted for BD8381EFV-M, which is optimized with the use of the recommended L value in the design stage. This recommendation is based upon the efficiency as well as the stability. The L values outside this recommended range may cause irregular switching waveform and hence deteriorate stable operation.
- n (efficiency) is approximately 80%

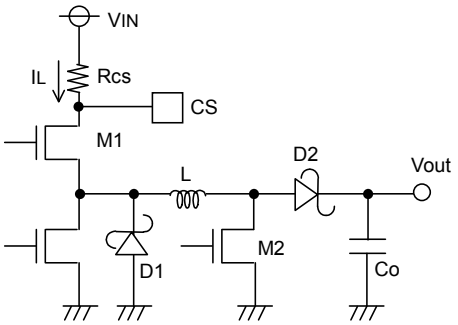


Fig.21 External Application Circuit

2. The setting of over-current protection

Choose Rcs with the use of the equation Vocp_min (=0.54V) / Rcs > IL_MAX

When investigating the margin, it is worth noting that the L value may vary by approximately ±30%.

3. The selection of the L

In order to achieve stable operation of the current-mode DC/DC converter, we recommend selecting the L value in the range indicated below:

$$0.05\ [V/\mu s] < \frac{Vout \times Rcs}{L} < 0.3\ [V/\mu s]$$

The smaller $\frac{Vout \times Rcs}{L}$ allows stability improvement but slows down the response time.

4. Selection of coil L, diode D1 and D2, MOSFET M1 and M2, and Rcs

	Current rating	Voltage rating	Heat loss
Coil L	> IL_MAX	—	
Diode D1	> Iocp	> VIN_MAX	
Diode D2	> Iocp	> Vout	
MOSFET M1	> Iocp	> VIN_MAX	
MOSFET M2	> Iocp	> Vout	
Rcs	—	—	> $Iocp^2$ × Rcs

※ Allow some margin, such as the tolerance of the external components, when selecting.

※ In order to achieve fast switching, choose the MOSFETs with the smaller gate-capacitance.

5. Selection of the output capacitor
Select the output capacitor Cout based on the requirement of the ripple voltage Vpp.

$$Vpp = \frac{Iout}{Cout} \times \frac{Vout}{Vout+VIN} \times \frac{1}{Fosc} + IL\_MIN \times RESR$$

Choose Cout that allows the Vpp to settle within the requirement. Allow some margin also, such as the tolerance of the external components.

6. Selection of the input capacitor
A capacitor at the input is also required as the peak current flows between the input and the output in DC/DC conversion. We recommend an input capacitor greater than 10μF with the ESR smaller than 100mΩ. The input capacitor outside of our recommendation may cause large ripple voltage at the input and hence lead to malfunction.

7. Phase Compensation Guidelines
In general, the negative feedback loop is stable when the following condition is met:
- Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 30º or more)

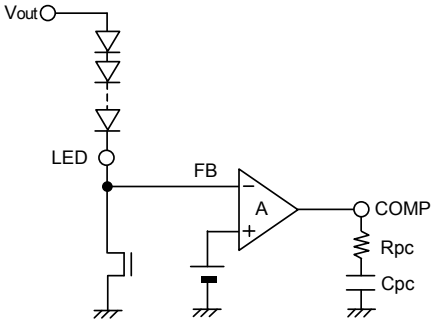
However, as the DC/DC converter constantly samples the switching frequency, the gain-bandwidth (GBW) product of the entire series should be set to 1/10 the switching frequency of the system. Therefore, the overall stability characteristics of the application are as follows:
- Overall gain of 1 (0dB) with a phase lag of less than 150º (i.e., a phase margin of 30º or more)
- GBW (frequency at gain 0dB) of 1/10 the switching frequency

Thus, to improve response within the GBW product limits, the switching frequency must be increased.

The key for achieving stability is to place fz near to the GBW. GBW is decided by phase delay fp1 by COUT and output impedance RL. Of each becomes like the next expression.

$$\text{Phase-lead} \quad fz = \frac{1}{2\pi CpcRpc} \ [Hz]$$

$$\text{Phase-lag} \quad fp1 = \frac{1}{2\pi RLCout} \ [Hz]$$



Good stability would be obtained when the fz is set between 1kHz～10kHz.
Please substitute the value at the maximum load for RL.

In buck-boost applications, Right-Hand-Plane (RHP) Zero exists. This Zero has no gain but a pole characteristic in terms of phase. As this Zero would cause instability when it is in the control loop, so it is necessary to bring this zero before the GBW.

$$fRHP = \frac{Vout+VIN/(Vout+VIN)}{2\pi I_{LOAD}L} \ [Hz]$$

I_{LOAD}: MAXIMUM LOAD CURRENT

It is important to keep in mind that these are very loose guidelines, and adjustments may have to be made to ensure stability in the actual circuitry. It is also important to note that stability characteristics can change greatly depending on factors such as substrate layout and load conditions. Therefore, when designing for mass-production, stability should be thoroughly investigated and confirmed in the actual physical design.

8. Setting of the soft-start
   The soft-start allows minimization of the coil current as well as the overshoot of the output voltage at the start-up.

   For the capacitance we recommend in the range of 0.001 ~ 0.1μF. For the capacitance less than 0.001μF may cause overshoot of the output voltage. For the capacitance greater than 0.1μF may cause massive reverse current through the parasitic elements of the IC and damage the whole device. In case it is necessary to use the capacitance greater than 0.1μF, ensure to have a reverse current protection diode at the Vcc or a bypass diode placed between the SS-pin and the Vcc.

   Soft-start time TSS

   TSS = CSSX0.7V / 5uA [s] CSS: The capacitance at the SS-pin

9. Verification of the operation by taking measurements
   The overall characteristic may change by load current, input voltage, output voltage, inductance, load capacitance, switching frequency, and the PCB layout. We strongly recommend verifying your design by taking the actual measurements.

●Power consumption calculation

$$Pc(N) = ICC*VCC + \frac{1}{2}*Ciss*VREG*Fsw*VREG \times 2 \times 2 + \frac{1}{2} \times Ciss \times VREG \times F_{PWM} \times VREG \times 2$$

ICC : Current of the maximum circuit
VCC : Power-supply voltage
Ciss : External FET capacity
Vsw : SW gate voltage
Fsw : SW frequency
F_{PWM} : PWM frequency

＜Calculation example＞
When assuming

$$Pc(4) = 10mA \times 30V + 500pF \times 5V \times 300kHz \times 5V \times 2 \times 2 + \frac{1}{2} \times 1500pF \times 5 \times 200 \times 5 \times 2,$$

it becomes
Pc = about 300mW.

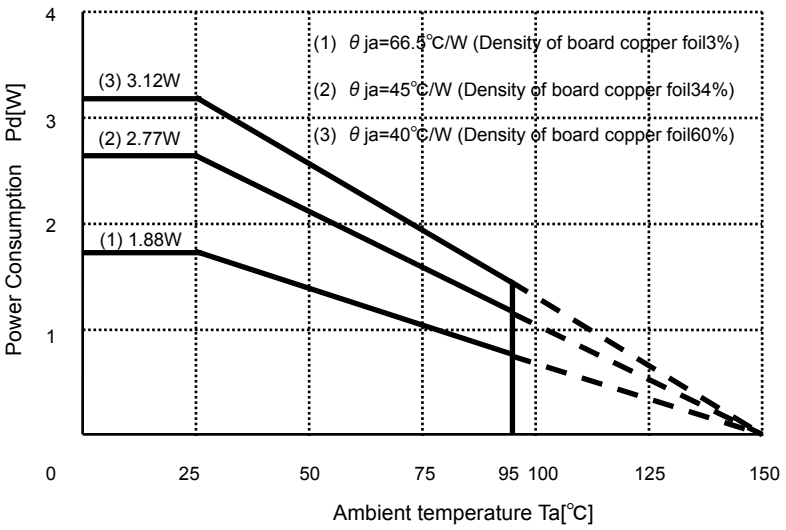


Fig.22

Note1: The value of Power consumption : on glass epoxy board measuring 70mm×70mm×1.6mm
(1 layer board/Copper foil thickness 18μm)
Note2: The value changes depending on the density of the board copper foil.
However, this value is an actual measurement value and no guarantee value.

Pd=2200mW (968mW) : Density of the board copper foil 3%
Pd=3200mW (1408mW) : Density of the board copper foil 34%
Pd=3500mW (1540mW) : Density of the board copper foil 60% The value in () is a Power consumption of the Ta=125℃.

●Application circuit 1

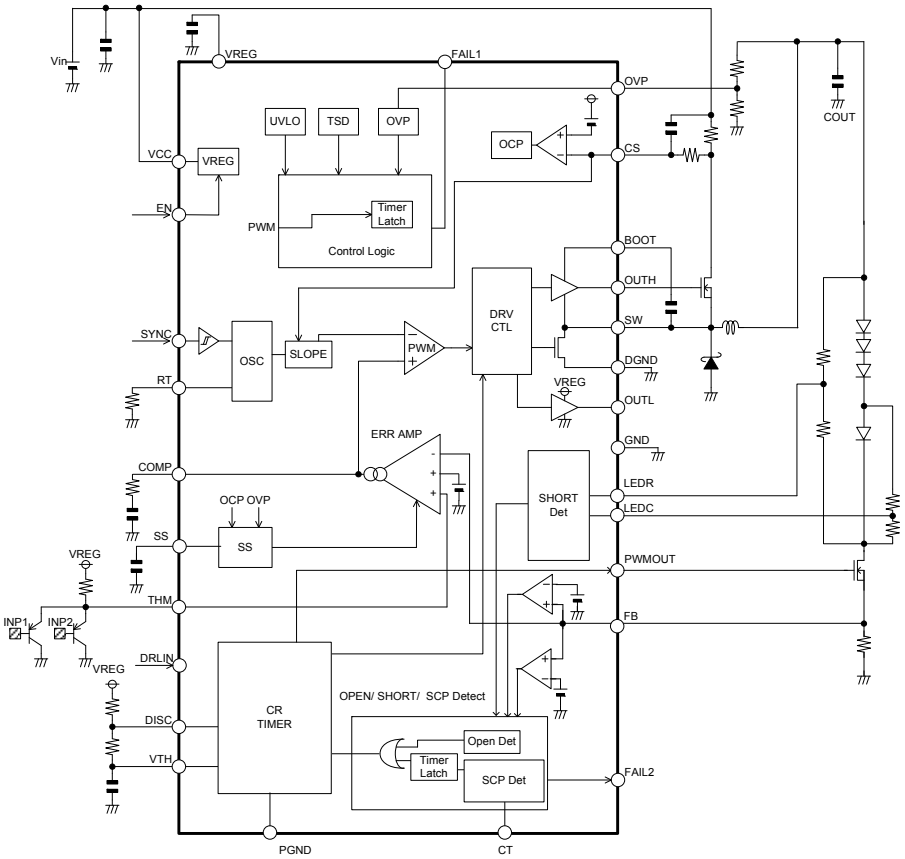


Fig. 23
Buck application composition (It is INP1, INP2, and two input selector function.)

●Application circuit 2

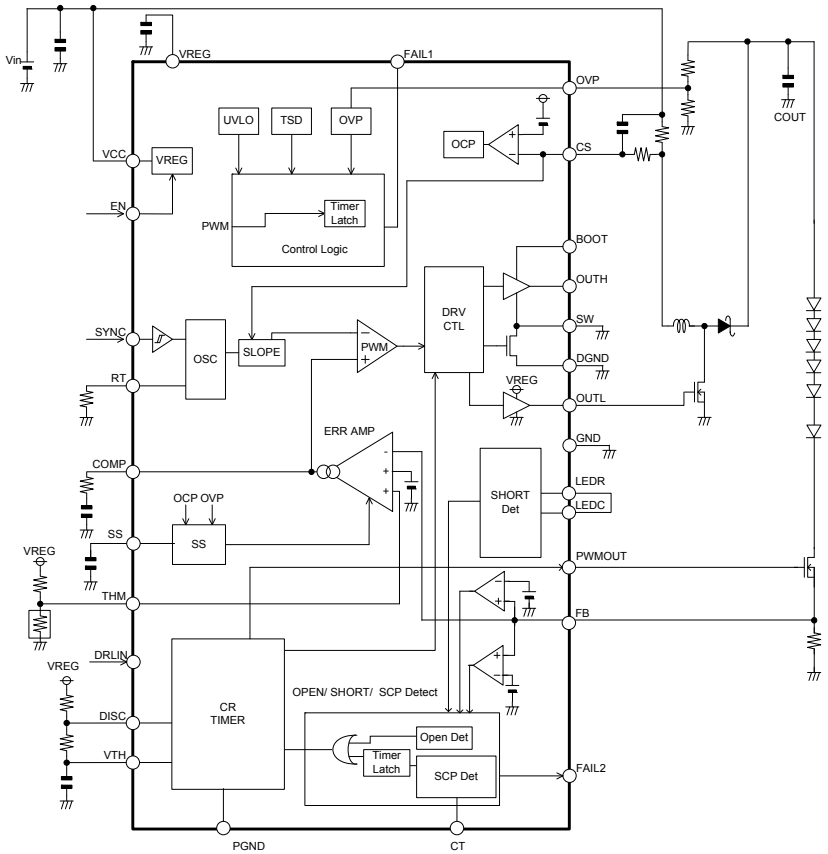
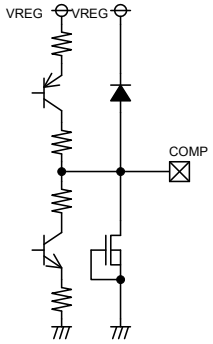
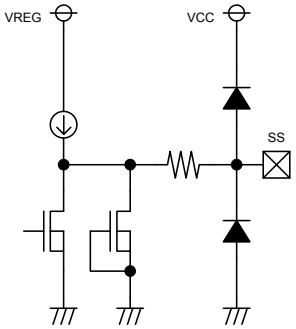
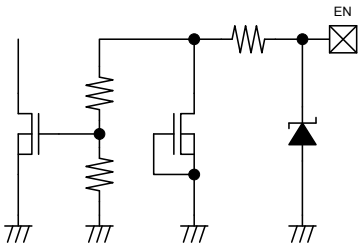
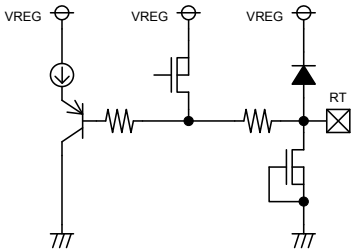
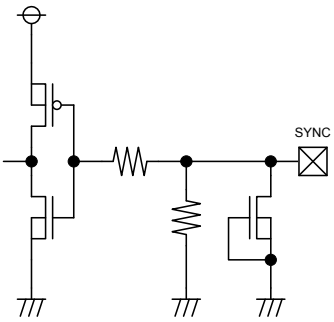
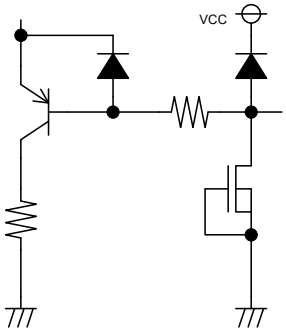
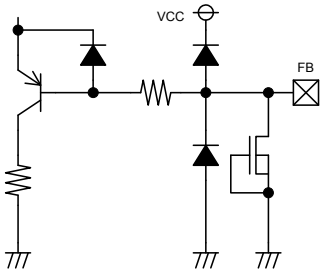
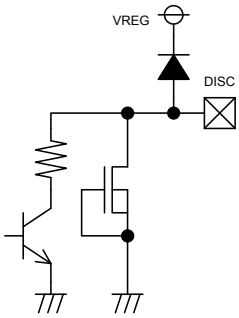
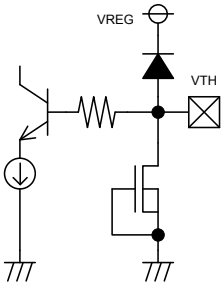
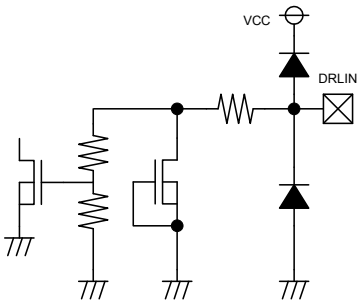
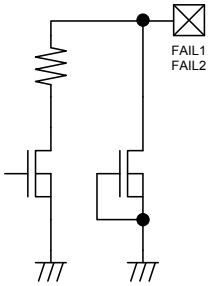
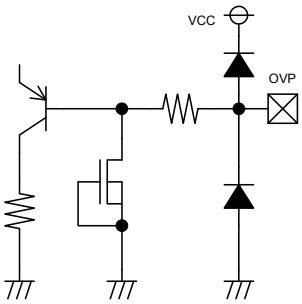


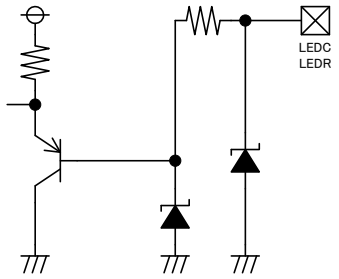
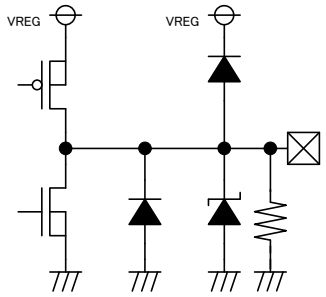
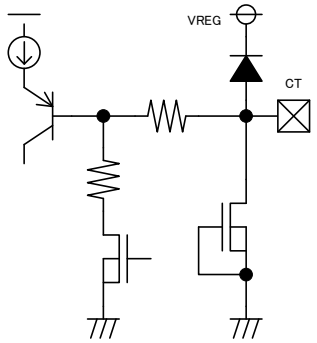
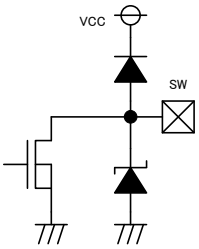
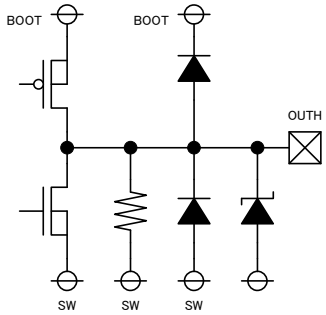
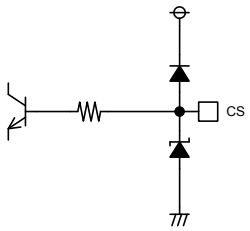
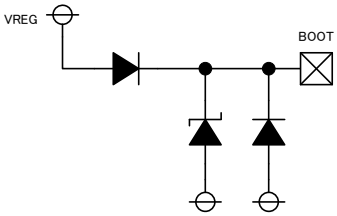
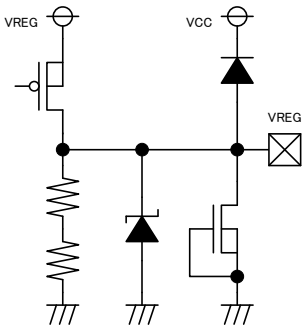
Fig. 24
Boost application composition (When invalidating short detection.)

●Input/output Equivalent Circuits

1. COMP	2. SS	4. EN
		
5. RT	**6. SYNC**	**8. THM**
		
9. FB	**10. DISC**	**11. VTH**
		
12. DRLIN	**13,14. FAIL1,FAIL2**	**15. OVP**
		

※The values are all Typ. value.

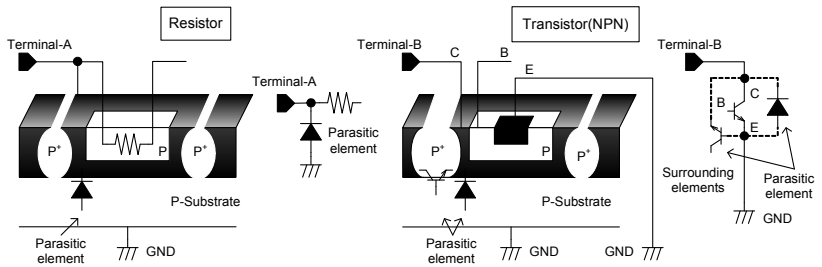
●Input/output Equivalent Circuits(Continuation)

16,17. LEDC, LEDR	19,22. PWMOUT, OUTL	20. CT
		
24. SW	**25. OUTH**	**26. CS**
		
27. BOOT	**28. VREG**	
		

※The values are all Typ. value.

●Notes for use

1. Absolute maximum ratings
   We are careful enough for quality control about this IC. So, there is no problem under normal operation, excluding that it exceeds the absolute maximum ratings. However, this IC might be destroyed when the absolute maximum ratings, such as impressed voltages or the operating temperature range(Topr), is exceeded, and whether the destruction is short circuit mode or open circuit mode cannot be specified. Please take into consideration the physical countermeasures for safety, such as fusing, if a particular mode that exceeds the absolute maximum rating is assumed.
2. Reverse polarity connection
   Connecting the power line to the IC in reverse polarity (from that recommended) will damage the part. Please utilize the direction protection device as a diode in the supply line.
3. Power supply line
   Due to return of regenerative current by reverse electromotive force, using electrolytic and ceramic suppress filter capacitors (0.1μF) close to the IC power input terminals (Vcc and GND) are recommended. Please note the electrolytic capacitor value decreases at lower temperatures and examine to dispense physical measures for safety. And, for ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, width of power wiring, GND wiring, and routing of wiring. Please make the power supply lines (where large current flow) wide enough to reduce the resistance of the power supply patterns, because the resistance of power supply pattern might influence the usual operation.
4. GND line
   The ground line is where the lowest potential and transient voltages are connected to the IC.
5. Thermal design
   Do not exceed the power dissipation (Pd) of the package specification rating under actual operation, and please design enough temperature margins.
6. Short circuit mode between terminals and wrong mounting
   Do not mount the IC in the wrong direction and be careful about the reverse-connection of the power connector. Moreover, this IC might be destroyed when the dust short the terminals between them or power supply, GND.
7. Radiation
   Strong electromagnetic radiation can cause operation failures.
8. ASO(Area of Safety Operation.)
   Do not exceed the maximum ASO and the absolute maximum ratings of the output driver.
9. TSD(Thermal shut-down)
   The TSD is activated when the junction temperature (Tj) reaches 175℃(with 25℃ hysteresis), and the output terminal is switched to Hi-z. The TSD circuit aims to intercept IC from high temperature. The guarantee and protection of IC are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.
10. Inspection by the set circuit board
    The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, please discharge electricity in each and all process. Moreover, in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transportation or preservation.
11. IC terminal input
    This IC is a monolithic IC, and has P^+ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is firmed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GND voltage potential is greater than the voltage potential at Terminals A or B, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND(P substrate). Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing.



structure of IC

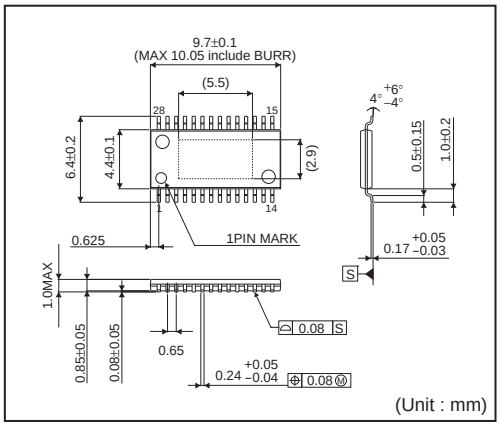
12. Earth wiring pattern
    Use separate ground lines for control signals and high current power driver outputs. Because these high current outputs that flows to the wire impedance changes the GND voltage for control signal. Therefore, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned

●Ordering part number

B	D	8	3	8	1	E	F	V	-	M	E	2

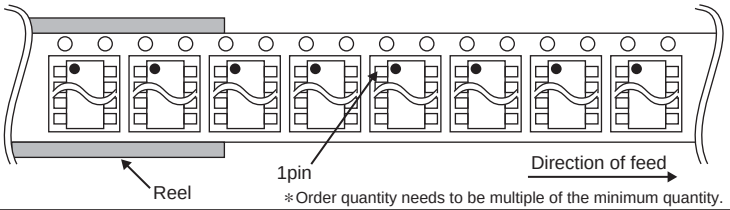
- Part No.
- Part No.
- Package EFV: HTSSOP-B28
- for Automotive
- Packaging and forming specification E2: Embossed tape and reel

HTSSOP-B28



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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